

## HIGH VOLTAGE TERMINATION WITH BURIED FIELD-SHAPING REGION

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

This Invention relates to improvements in semiconductor devices and methods, and more particularly to improvements in methods and structures for increasing the breakdown voltage of junctions in termination regions of semiconductor devices, and the like, of the type in which junction breakdown voltages are relatively high, for example, in the range above about 60–100 volts, and to methods for making same.

#### 2. Relevant Background

Within the past few years, a dramatic change has taken place in the power semiconductor industry. Through the use of new or improved device structures and technology, MOS transistors have been modified to provide high currents and high voltages. When such devices are used in association with an integrated control circuit in the same chip a very compact and efficient device is provided that is particularly advantageous, compared with separate components.

However, a recurring problem in providing such power devices is maximizing their breakdown voltage. The breakdown mechanisms in power MOS transistors can be caused by at least four mechanisms. An “avalanche breakdown” occurs when the electric field in the semiconductor accelerates carrier into atoms having bound electrons with sufficient energy to generate electron-hole pairs. These carriers are in turn accelerated by the field, resulting in further electron-hole pair production and high currents. A “Zener breakdown” occurs when the electric field is sufficiently high that carriers gain enough energy to tunnel through the junction potential barrier. A “punch-through breakdown” occurs when the depletion region of a reverse-biased junction spreads to another junction in the vicinity, connecting the two junctions by a continuous region and allowing current to flow from one junction to the other. A “dielectric breakdown” occurs when the electric field in a dielectric layer exceeds its dielectric strength, allowing a large current flow through the dielectric, usually permanently destroying it. The avalanche breakdown mechanism is of primary interest herein, as the Zener, punch-through, and dielectric breakdown mechanisms are usually minimized in a properly designed device.

In this light, in the context of an MOS device, the breakdown voltage is a decreasing function of the dopant concentration in the drain region of the power device, and is an increasing function of the curvature radius of the body/drain junction therein. To date, the problem has been addressed by appropriate terminations of this junction. In the construction of discrete or integrated VDMOS transistors, the breakdown voltage, which should be as high as possible, and the ON-resistance of the device, which should be as low as possible, are simultaneously optimized. The optimization of these two basic parameters depends on the adoption of an edge configuration apt to achieve a breakdown voltage as close as possible to the theoretical breakdown voltage of a planar junction with an infinite radius of curvature of its perimeter in the direction of the depth of the junction. Such a junction is often referred to as a “plane” junction.

Typical terminations include, for example, dielectric or metallic field plates, floating or field limiting rings, low dopant concentration regions, and so forth. A review of some of these techniques can be found in A. Blicher, *Field-Effect and Bipolar Power Transistor Physics*, Academic Press, pp.

53–84, 1981, and in “POWER INTEGRATED CIRCUITS: Physics, Design, and Applications” Antognetti, McGraw-Hill Book Company, (1986), pp. 3.1–3–58.

A side cross sectional view of a portion of a terminating structure **10** of the type that uses floating surface rings to achieve a high voltage breakdown is shown in FIG. **1**. The terminating structure **10** is formed in an epitaxial layer **12** which is lightly doped with a donor impurity to provide the N- epitaxial layer shown. A device region **14** (such as a body region of a vertical power DMOS device, or the like) is formed in the epitaxial layer **12** of highly doped acceptor type impurities to provide a P+ region, as known in the art.

A number of rings **16–19** are provided encircling the associated semiconductor device at the surface of the epitaxial layer **12**. The rings **16–19** are spaced concentrically outwardly from the semiconductor device (not completely shown) at its lateral edge or periphery within the epitaxial layer **12**. A dielectric layer **22** overlies the rings **16–19** and the epitaxial layer **12** to isolate them from the structures formed thereover. Metal region **24** provides electrical contact to the device region **14**, while metal region **26** is the conductor that terminates the high field region.

Another technique that has been used to terminate semiconductor devices is shown by the structure shown in the side cross-sectional view of FIG. **2**, in which progressively shallower, lightly doped rings **32** and **34** are used to achieve a high breakdown voltage. More specifically, the adjacent concentric rings **32** and **34** are formed in the epitaxial layer **36** at surface regions adjacent to a region **38** of an semiconductor device (not completely shown).

The device region **38** is constructed with an acceptor type impurity to provide a P+ region, and, similarly, concentric lightly doped rings **32** and **34** are doped with lighter doses of acceptor impurities to provide P- and P-- regions, respectively. An overlying dielectric region **40** is provided over the surface regions of the device region **38**, lightly doped rings **32** and **34**, and epitaxial layer **36**, and metal contact **44** is provided to establish electrical contact to the device **38** while metal region **46** is the conductor that terminates the high field region.

As shown in FIG. **3**, a side cross-sectional view of another structure **50** is shown for terminating a semiconductor device. The structure **50** uses a single, deep lightly doped ring **52** to insure a high breakdown voltage. The deep lightly doped ring **52** is formed adjacent to the device region **54**, both being formed at the surface of the epitaxial layer **56**, which is lightly doped with a donor impurity. In the embodiment shown, both the device region **54** and lightly doped ring **52** are doped with an acceptor type impurity.

A dielectric layer **58** is formed over the surface areas of the device region **54**, lightly doped ring **52**, and epitaxial region **56**, as shown, and metal contact **60** is provided to contact the device region **54** while metal region **62** is the conductor that terminates the high field region.

Still another embodiment of a known termination structure **70** is shown in the side cross-sectional view of FIG. **4**, in which the terminating structure **70** includes a plurality of deep, lightly doped rings **72** and **74** at the surface of the epitaxial region **78** to achieve a high breakdown voltage. The structure **70** is similar to the structure **30** described above with respect to FIG. **2**, except for the depth of the lightly doped rings **72** and **74** adjacent the device **76**.

A dielectric layer **80** overlies the surface regions of the lightly doped rings **72** and **74**, as well as portions of the device **76** and substrate **78**. Metal contact **82** is provided to the device **76** while metal region **84** is the conductor that terminates the high field region.